

# Cree 600 V Schottky Diode *Z-REC<sup>TM</sup>* Rectifiers

## Qualification Report

### Summary

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This report documents the qualification and reliability test results for the *Z-Rec<sup>TM</sup>* Cree 600-V Schottky diode product family. This report also describes the test methods and criteria used for certifying a qualified process.

This report certifies that Schottky diode die manufactured at Cree, Inc., Durham, North Carolina, USA, which are voltage breakdown rated at 600 V, current-rated at or below 20 A, and are fabricated using nominally 100 mm (or smaller) SiC substrates manufactured by Cree, Inc., to be production qualified. Furthermore, this report certifies that product families using 600-V SiC Schottky diode die assembled in TO-220 standard, TO-220 "Full Pack," TO-252 "DPAK," TO-263 "D2PAK" and TO-247 package styles to be production qualified. Surface-mount devices have been qualified to MSL-3.

In total, 6972 devices were evaluated in a variety of qualification and reliability stress tests across the various current ratings and package styles available for the 600-V Schottky diode product line.

Of these, there were zero failures during qualification testing.



## Table of Contents

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<b>Summary</b> .....	<b>1</b>
<b>Table Of Contents</b> .....	<b>2</b>
<b>Qualification Test Plan</b> .....	<b>3</b>
Parametric Verification.....	3
External Visual Inspection.....	3
Autoclave.....	3
H3TRB.....	3
HTRB.....	3
Temperature Cycle.....	3
Intermittent Operating Life.....	3
ESD-HBM.....	3
ESD-CDM.....	3
ESD-MM.....	3
<b>Sampling Plan</b> .....	<b>4</b>
<b>Failure Criteria</b> .....	<b>4</b>
<b>Definition of a Qualification Family</b> .....	<b>4</b>
<b>Qualification Test Descriptions and Results</b> .....	<b>5</b>
Parametric Verification.....	5
External Visual Inspection.....	6
Autoclave.....	6
H3TRB.....	7
HTRB.....	8
Temperature Cycle.....	9
Intermittent Operating Life.....	10
ESD-HBM.....	11
ESD-CDM.....	11
ESD-MM.....	12
DHTRB.....	12
<b>MSL Testing</b> .....	<b>13</b>
<b>Reliability Testing and Failure Mode Analysis</b> .....	<b>14</b>
Three-Temperature Life Testing.....	14
Electric-Field and Moisture Accelerated Life testing.....	15
<b>Field Reliability and Failure Rate</b> .....	<b>16</b>
<b>Conclusion</b> .....	<b>16</b>



## Qualification Test Plan

The product-qualification test plan is outlined in Table 1. This plan is based on the guidelines of JESD47-B, *Stress-Test-Driven Qualification of Integrated Circuits*, Published by the *Jedec Solid State Technology Association*, and AEC-Q101-REV-C, *Stress Test Qualification for Automotive Grade Discrete Semiconductors*.

**Table 1: 600-V Schottky Diode Product Qualification Test Plan**  
( $T_c$  = case temperature,  $T_j$  = junction temperature,  $V_{br}$  = breakdown voltage)

Test	Stress	Duration	Sample Size	Reference
<b>Parametric Verification</b>	Evaluate Data Sheet Specifications	N/A	3 lots x 25 devices (75 total)	AEC-Q101-C
<b>External Visual Inspection</b>	Observe External Surfaces and Markings	N/A	All devices used for qualification	AEC-Q101-C
<b>Autoclave</b>	Moisture, Thermal, Pressure 100%RH, 121°C, 205kPa	96h	3 lots x 25 devices (75 total)	JESD22-A102-B Condition C
<b>H3TRB</b>	Bias, Moisture 100V 85C/85%RH	1000h	3 lots x 77 devices (231 total)	JESD22-A101-B
<b>HTRB</b>	Bias, Thermal 100% $V_{br}$ $T_c=175^\circ\text{C}$	500h	3 lots x 77 devices (231 total)	AEC-Q101-REV-C
<b>Temperature Cycle</b>	Thermal, Mechanical -55°C to 150°C 1000 cycles	1 minute soak, 15°C/min ramp rate 2 cycles per hour	3 lots x 77 devices (231 total)	JESD22-A104-B Condition H Soak mode 1
<b>Intermittent Operating Life</b>	Bias, Thermal $\Delta T_j(\text{min})$ 100°C	Product dependent*	3 lots x 77 devices (231 total)	JESD22-A105-C and AEC-Q101-C
<b>ESD-HBM</b>	Electric Field	5 cycles/terminal	1 lot, 30 devices (30 total)	AEC-Q101-001
<b>ESD-CDM</b>	Electric Field	5 cycles/terminal	1 lot, 30 devices (30 total)	AEC-Q101-005
<b>ESD-MM</b>	Electric Field	5 cycles/terminal	1 lot, 30 devices (30 total)	AEC-Q101-002

\*Duration and number of cycles is product-dependent, as described in AEC-Q101-REV-C and Table 7 of this document.



## Sampling Plan

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Random sampling procedures are used to select devices to be evaluated in the various product-qualification tests on Table 1. Sample size meets or exceeds the recommendations of JEDEC standards JESD47B and AEC-Q101-REV-C for qualification of a product family where generic data may be used. For component-specific qualifications, the three-lot sample size (where specified in Table 1) is reduced to one lot. For low volume or high cost parts, the sample size per test may be reduced from 77 to 25, as appropriate.

## Failure Criteria

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A device failure is defined as a condition in which a stressed device can no longer meet its data sheet specifications or has consequential external physical damage attributable to an environmental test.

A determination of root cause will be made immediately for any failure found. If the root cause of failure is mishandling, test-equipment failure, or a data-acquisition failure, the failing devices will be removed from the test and not counted as a qualification failure. If time constraints regarding test suspension are not violated, the qualification test will resume with the remaining devices so long as the total number of remaining devices is at least 90% of the starting sample size (per lot).

A single failure that cannot be identified within the time constraint for a suspended test, or is identified as an inherent device failure, will constitute a qualification failure for the test at hand and noted in the final qualification report. Other qualification tests may proceed so long as their results are not likely to be significantly impacted by the corrective action required by the identified failure mode. This determination will be made by the reliability manager responsible for the product qualification.

## Definition of a Qualification Family

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A qualification family is defined as meeting all of the following criteria:

1. A single process technology (Schottky diode, MOSFET, p-n junction diode, BJT, JFET, etc.)
2. A single fab process (same design rules, process flow, number of masks and lithographic process, cell density, doping process and dopant type, epi process and thickness, substrate process and thickness, passivation material and thickness, oxidation process and thickness, front/back metal materials, thicknesses, and number of levels)
3. A single fab site
4. A single package assembly site
5. A single package type (TO-220, TO-247, TO-252, TO-263, etc.)
6. A single assembly process (leadframe base material, leadframe plating, die attach material and method, wirebond material and method, mold compound or other encapsulation material)



## Qualification Test Descriptions and Results

### Parametric Verification

Parametric Verification (PV) is used to evaluate whether the devices tested meet performance specifications as listed on the product data sheet. The Process Capability Index ( $C_{pk}$ ) is calculated to determine whether the total variation in the process meets customer quality requirements. Results are shown in Table 2(a-f).

**Table 2a: Parametric Verification Results C3D10060A at 25°C**

TEST NAME	UNIT	SPEC LSL	SPEC USL	MIN	MAX	MEAN	STD.DEV.	CPK
VF (Rated Current)	V		1.8	1.4	1.7	1.5	0.02	4.4
IR at 600 V	μA		50	0.5	15.0	6.3	3.6	4.1
VBR at 80 μA	V	600		675	1060	824	81	1.6

**Table 2b: Parametric Verification Results C3D10060A at 175°C**

TEST NAME	UNIT	SPEC LSL	SPEC USL	MIN	MAX	MEAN	STD.DEV.	CPK
VF (Rated Current)	V		2.4	1.90	2.35	2.05	0.06	1.9
IR at 600 V	μA		200	4.4	95.3	43.8	30.2	1.7
VBR at 1000 μA	V	600		925	1422	1231	94	2.2

**Table 2c: Parametric Verification Results C3D10060A at -55°C**

TEST NAME	UNIT	SPEC LSL	SPEC USL	MIN	MAX	MEAN	STD.DEV.	CPK
VF (Rated Current)	V		2.1	1.7	1.9	1.7	0.04	2.7
IR at 600 V	μA		50	0.04	2.0	0.2	0.4	38.7
VBR at 80 μA	V	600		816	999	946	46	2.5

**Table 2d: Parametric Verification Results C3D04060A at 25°C**

TEST NAME	UNIT	SPEC LSL	SPEC USL	MIN	MAX	MEAN	STD.DEV.	CPK
VF (Rated Current)	V		1.8	1.5	1.7	1.5	0.04	2.1
IR at 600 V	μA		50	0.7	1.7	1.1	1.1	14.4
VBR at 1000 μA	V	600		801	982	917	42	2.5

**Table 2e: Parametric Verification Results C3D04060A at 175°C**

TEST NAME	UNIT	SPEC LSL	SPEC USL	MIN	MAX	MEAN	STD.DEV.	CPK
VF (Rated Current)	V		2.4	1.8	2.1	2.0	0.1	2.4
IR at 600 V	μA		100	1.3	10.6	3.0	1.9	17.3
VBR at 80 μA	V	600		806	1016	936	49	2.3

**Table 2f: Parametric Verification Results C3D04060A at -55°C**

TEST NAME	UNIT	SPEC LSL	SPEC USL	MIN	MAX	MEAN	STD.DEV.	CPK
VF (Rated Current)	V		2.1	1.7	1.9	1.8	0.1	1.9
IR at 600 V	μA		50	0.04	2.0	0.4	0.4	36.9
VBR at 1000 μA	V	600		809	1000	930	47	2.3

A  $C_{pk}$  of 1.33 (or above) is considered indicative of a process that is statistically well in control. Values for specific products are available upon request.



**External Visual**

External visual (EV) inspection is used to identify external defects associated with the device package. Markings, construction and workmanship are evaluated with the unaided eye or with up to a 30X magnification, as appropriate for the device feature under inspection.

No visual anomalies were observed during external visual inspection on any of the die used for qualification.

**Autoclave**

Autoclave testing is used to evaluate the moisture resistance of non-hermetic packaged devices. The device under test (DUT) is unbiased. Autoclave testing is used to identify failure mechanisms internal to the package, such as delamination and corrosion.

External inspection detected no defects after autoclave stressing. No internal defects were observed during Destructive Physical Analysis (DPA). No electrical failures were observed. Results are shown in Table 3.

**Table 3: Autoclave Test Results**

Result	Cree Part #	TEST DESCRIPTION	TEST CONDITIONS	LOTS	TESTED	FAILED
Pass	C3D02060A C3D02060F C3D04060A C3D04060F C3D10060A C3D10060F C3D20060D	External Visual	Per spec	17	425	0
Pass	C3D02060A	Autoclave	Ta = 121°C,P=205kPa, RH=100%	1	25	0
Pass	C3D02060F	Autoclave	Ta = 121°C,P=205kPa, RH=100%	1	25	0
Pass	C3D04060A	Autoclave	Ta = 121°C,P=205kPa, RH=100%	3	75	0
Pass	C3D04060F	Autoclave	Ta = 121°C,P=205kPa, RH=100%	3	75	0
Pass	C3D10060A	Autoclave	Ta = 121°C,P=205kPa, RH=100%	3	75	0
Pass	C3D10060F	Autoclave	Ta = 121°C,P=205kPa, RH=100%	3	75	0
Pass	C3D20060D	Autoclave	Ta = 121°C,P=205kPa, RH=100%	3	75	0
Pass	C3D02060A C3D02060F C3D04060A C3D04060F C3D10060A C3D10060F C3D20060D	DPA	Per spec	17	425	0



**H3TRB**

High-humidity, high-temperature reverse bias (H3TRB) testing is used to evaluate the reliability of the DUT in humid environments. The DUT is biased at 80% of rated voltage. H3TRB is designed to accelerate moisture-related failure modes, including internal corrosion, internal oxidation and dendritic growth.

External inspection detected no defects after H3TRB stressing. No internal defects were observed during DPA. No electrical failures were observed. Results are shown in Table 4.

**Table 4: H3TRB Test Results**

Result	Cree Part #	TEST DESCRIPTION	TEST CONDITIONS	LOTS	TESTED	FAILED
Pass	C3D02060A C3D02060F C3D04060A C3D04060F C3D10060A C3D10060F C3D20060D	External Visual	Per spec	17	1205	0
Pass	C3D02060A	H3TRB	Ta = 85°C,V=480V, RH=85%	1	25	0
Pass	C3D02060F	H3TRB	Ta = 85°C,V=480V, RH=85%	1	25	0
Pass	C3D04060A	H3TRB	Ta = 85°C,V=480V, RH=85%	3	231	0
Pass	C3D04060F	H3TRB	Ta = 85°C,V=480V, RH=85%	3	231	0
Pass	C3D10060A	H3TRB	Ta = 85°C,V=480V, RH=85%	3	231	0
Pass	C3D10060F	H3TRB	Ta = 85°C,V=480V, RH=85%	3	231	0
Pass	C3D20060D	H3TRB	Ta = 85°C,V=480V, RH=85%	3	231	0
Pass	C3D02060A C3D02060F C3D04060A C3D04060F C3D10060A C3D10060F C3D20060D	DPA	Per spec	17	1205	0



**HTRB**

High-temperature reverse-bias (HTRB) testing is used to determine the breakdown robustness of devices under high field and temperature conditions. For 600-V products, the DUT is biased at 100% of its maximum operating static DC field conditions at a flange temperature equal to its maximum static DC forward-operating junction temperature. HTRB is designed to hasten field-accelerated failure modes and early-life failures due to fabrication errors.

External inspection detected no defects after HTRB stressing. No internal defects were observed during DPA. No electrical failures were observed. Results are shown in Table 5.

**Table 5: HTRB Test Results**

Result	Cree Part #	TEST DESCRIPTION	TEST CONDITIONS	LOTS	TESTED	FAILED
Pass	C3D02060A C3D02060F C3D04060A C3D04060F C3D10060A C3D10060F C3D20060D	External Visual	Per spec	17	1205	0
Pass	C3D02060A	HTRB	Ta = 175°C,V=600V	1	25	0
Pass	C3D02060F	HTRB	Ta = 175°C,V=600V	1	25	0
Pass	C3D04060A	HTRB	Ta = 175°C,V=600V	3	231	0
Pass	C3D04060F	HTRB	Ta = 175°C,V=600V	3	231	0
Pass	C3D10060A	HTRB	Ta = 175°C,V=600V	3	231	0
Pass	C3D10060F	HTRB	Ta = 175°C,V=600V	3	231	0
Pass	C3D20060D	HTRB	Ta = 175°C,V=600V	3	231	0
Pass	C3D02060A C3D02060F C3D04060A C3D04060F C3D10060A C3D10060F C3D20060D	DPA	Per spec	17	1205	0



### Temperature Cycle

Temperature cycling is used to determine the robustness of devices and interconnects when exposed to alternating high- and low-temperature extremes. The DUT is unbiased. Temperature cycling is used to identify failure modes that result from coefficient of thermal expansion (CTE) mismatch between materials and similar thermo-mechanical phenomena.

External inspection detected no defects after temperature-cycle stressing. No internal defects were observed during DPA. No electrical failures were observed. Results are shown in Table 6.

**Table 6: Temperature Cycle Test Results**

Result	Cree Part #	TEST DESCRIPTION	TEST CONDITIONS	LOTS	TESTED	FAILED
Pass	C3D02060A C3D02060F C3D04060A C3D04060F C3D10060A C3D10060F C3D20060D	External Visual	Per spec	17	1205	0
Pass	C3D02060A	TC	T_low=-55°C,T_high=+150°C	1	25	0
Pass	C3D02060F	TC	T_low=-55°C,T_high=+150°C	1	25	0
Pass	C3D04060A	TC	T_low=-55°C,T_high=+150°C	3	231	0
Pass	C3D04060F	TC	T_low=-55°C,T_high=+150°C	3	231	0
Pass	C3D10060A	TC	T_low=-55°C,T_high=+150°C	3	231	0
Pass	C3D10060F	TC	T_low=-55°C,T_high=+150°C	3	231	0
Pass	C3D20060D	TC	T_low=-55°C,T_high=+150°C	3	231	0
Pass	C3D02060A C3D02060F C3D04060A C3D04060F C3D10060A C3D10060F C3D20060D	DPA	Per spec	17	1205	0



**Intermittent Operating Life**

Intermittent Operating Life (IOL) testing is designed to hasten thermally accelerated failure modes (under bias) and early-life failures due to CTE mismatch and assembly defects. The DUT is switched from forward bias to zero bias in specific time intervals to achieve a change in junction temperature ( $T_j$ ) of 100°C or greater. Table 7 details the time intervals to be used.

**Table 7 :IOL Test Conditions**

Package Type	Number of cycles (change in $T_j$ greater than or equal to 100°C)	Number of cycles (change in $T_j$ greater than or equal to 125°C)	Time per cycle (seconds)
Small (e.g., SMD SOTS)	15,000	7,500	120 on / 120 off
Medium (e.g., TO-220)	8,572	4,286	210 on / 210 off
Large (e.g., TO-247)	6,000	3,000	300 on / 300 off

External inspection detected no unexpected defects after IOL stressing. No internal defects were observed during DPA. No electrical failures were observed. Results are shown in Table 8.

**Table 8 :IOL Test Results**

Result	Cree Part #	TEST DESCRIPTION	TEST CONDITIONS	LOTS	TESTED	FAILED
Pass	C3D02060A C3D02060F C3D04060A C3D04060F C3D10060A C3D10060F C3D20060D	External Visual	Per spec	17	1205	0
Pass	C3D02060A	IOL	Per spec	1	25	0
Pass	C3D02060F	IOL	Per spec	1	25	0
Pass	C3D04060A	IOL	Per spec	3	231	0
Pass	C3D04060F	IOL	Per spec	3	231	0
Pass	C3D10060A	IOL	Per spec	3	231	0
Pass	C3D10060F	IOL	Per spec	3	231	0
Pass	C3D20060D	IOL	Per spec	3	231	0
Pass	C3D02060A C3D02060F C3D04060A C3D04060F C3D10060A C3D10060F C3D20060D	DPA	Per spec	17	1205	0



**ESD-HBM**

Electrostatic Discharge (ESD) – Human Body Model (HBM) testing is used to determine the electrostatic discharge threshold above which damage occurs in the device under test. HBM is meant to simulate an ESD event that occurs when a human body acquires charge and transfers that charge to a device during manual device handling or assembly. A standardized circuit is used to apply a specified waveform to the device, and the results dictate an ESD-HBM classification. Results are shown in Table 9.

All Cree Schottky diode products meet the following HBM classifications: AECQ101-001/ANSI ESD-STM5.1 Classification 3B (>8000 V), JEDEC/EIA JESD22 A114-D Classification 3B (>8000 V).

**Table 9 :ESD-HBM Test Results**

Result	Cree Part #	TEST DESCRIPTION	TEST CONDITIONS	LOTS	TESTED
Pass	C3D02060A	ESD-HBM	8000V	1	30
Pass	C3D02060E	ESD-HBM	8000V	1	30
Pass	C3D04060A	ESD-HBM	8000V	1	30
Pass	C3D04060F	ESD-HBM	8000V	1	30
Pass	C3D06060A	ESD-HBM	8000V	1	30
Pass	C3D06060G	ESD-HBM	8000V	1	30
Pass	C3D08060A	ESD-HBM	8000V	1	30
Pass	C3D10060A	ESD-HBM	8000V	1	30
Pass	C3D10060F	ESD-HBM	8000V	1	30
Pass	C3D20060D	ESD-HBM	8000V	1	30

**ESD-CDM**

Electrostatic Discharge (ESD) – Charged Device Model (CDM) testing is used to determine the electrostatic discharge threshold above which damage occurs in the device under test. CDM is meant to simulate an ESD event that occurs when triboelectric charge transfers to a device during manual device handling, assembly or product packaging. A standardized circuit is used to apply a specified waveform to the device, and the results dictate an ESD-CDM classification. Results are shown in Table 10.

All Cree Schottky diode products meet the following CDM classifications: ANSI ESD-DS5.3 Classification C5 (>1000 V), JEDEC/EIA JESD22 C101-C Classification IV (>1000 V).

**Table 10 :ESD-CDM Test Results**

Result	Cree Part #	TEST DESCRIPTION	TEST CONDITIONS	LOTS	TESTED
Pass	C3D02060A	ESD-CDM	1000V	1	30
Pass	C3D02060E	ESD-CDM	1000V	1	30
Pass	C3D04060A	ESD-CDM	1000V	1	30
Pass	C3D04060F	ESD-CDM	1000V	1	30
Pass	C3D06060A	ESD-CDM	1000V	1	30
Pass	C3D06060G	ESD-CDM	1000V	1	30
Pass	C3D08060A	ESD-CDM	1000V	1	30
Pass	C3D10060A	ESD-CDM	1000V	1	30
Pass	C3D10060F	ESD-CDM	1000V	1	30
Pass	C3D20060D	ESD-CDM	1000V	1	30



**ESD-MM**

Electrostatic Discharge (ESD) – Machine Model (MM) testing is used to determine the electrostatic discharge threshold above which damage occurs in the device under test. MM is meant to simulate an ESD event that occurs when an object transfers a charge to a device through a very low resistance path. A standardized circuit is used to apply a specified waveform to the device, and the results dictate an ESD-MM classification. Results are shown in Table 11.

All Cree Schottky diode products meet the following MM classifications: AECQ101-002/ANSI ESD-S5.2 Classification M4 (>400 V), JEDEC/EIA JESD22 A115-A Classification C (>400 V).

**Table 11: ESD-CDM Test Results**

Result	Cree Part #	TEST DESCRIPTION	TEST CONDITIONS	LOTS	TESTED
Pass	C3D02060A	ESD-MM	1000V	1	30
Pass	C3D02060E	ESD-MM	1000V	1	30
Pass	C3D04060A	ESD-MM	1000V	1	30
Pass	C3D04060F	ESD-MM	1000V	1	30
Pass	C3D06060A	ESD-MM	1000V	1	30
Pass	C3D06060G	ESD-MM	1000V	1	30
Pass	C3D08060A	ESD-MM	1000V	1	30
Pass	C3D10060A	ESD-MM	1000V	1	30
Pass	C3D10060F	ESD-MM	1000V	1	30
Pass	C3D20060D	ESD-MM	1000V	1	30

**DHTRB**

Dynamic HTRB (DHTRB) stresses the part in the same manner as HTRB, but the bias is switched from 100% of rated reverse bias to zero at 10.4kHz and a 50% duty cycle. The purpose of DHTRB is to accelerate failures driven by the increased leakage current that is present under transient conditions. To further accelerate the test, DHTRB is performed at 200°C to maximize thermally generated leakage. DHTRB is not included in the qualification test plan since it is not a standardized test. However, the results are mentioned here for completeness. Four hundred and sixty-two samples of C3D10060A and C3D06060A were used for DHTRB testing. Results are shown in Table 12.

External inspection detected no defects after 1000-hour DHTRB stressing. No internal defects were observed during DPA. No electrical failures were observed.

**Table 12: DHTRB Test Results**

Result	Cree Part #	TEST DESCRIPTION	TEST CONDITIONS	LOTS	TESTED	FAILED
Pass	C3D06060A	DHTRB	Ta=200°C,V=600V,f=10.4kHz, D=50%	3	231	0
Pass	C3D10060A	DHTRB	Ta=200°C,V=600V,f=10.4kHz, D=50%	3	231	0
Pass	C3D06060A C3D10060A	DPA	Per Spec	6	54	0



## MSL Testing

Moisture Sensitivity Level (MSL) testing is intended to classify non-hermetic surface mount devices (SMD) according to their sensitivity to damage during solder reflow operations. Damage may be due to absorbed moisture during storage and handling, thermal stresses inherent to the reflow operation itself, or the increase in vapor pressure of moisture inside the package during reflow operations.

MSL testing is conducted for Surface Mount Devices (SMD) according to the guidelines set forth in J-STD-020C, "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices" up to MSL Class 3, indicating a "floor life" of 168 hours at or below 30°C, 60%RH. Peak reflow temperature classification was 245°C, as specified by J-STD-020C for a SnPb eutectic die attach process. MSL classification applies to products using TO-252-2 (DPAK) and TO-263-2 (D2PAK) package types. The highest current rated die for a given package type was used for the evaluation (CSD10060G and CSD04060E). Results are shown in Table 13.

**Table 13 :MSL-3 Test Results**

Result	Cree Part #	TEST DESCRIPTION	TEST CONDITIONS	LOTS	TESTED	FAILED
Pass	CSD04060E CSD10060G	External Visual	Per spec	10	770	0
Pass	CSD04060E	Autoclave	Ta = 121°C,P=205kPa, RH=100%	1	77	0
Pass	CSD10060G	Autoclave	Ta = 121°C,P=205kPa, RH=100%	1	77	0
Pass	CSD04060E	HTRB	Ta = 175°C,V=600V	1	77	0
Pass	CSD10060G	HTRB	Ta = 175°C,V=600V	1	77	0
Pass	CSD04060E	H3TRB	Ta = 85°C,V=480V, RH=85%	1	77	0
Pass	CSD10060G	H3TRB	Ta = 85°C,V=480V, RH=85%	1	77	0
Pass	CSD04060E	TC	T_low=-55°C,T_high=+150°C	1	77	0
Pass	CSD10060G	TC	T_low=-55°C,T_high=+150°C	1	77	0
Pass	CSD04060E	IOL	Per spec	1	77	0
Pass	CSD10060G	IOL	Per spec	1	77	0
Pass	CSD04060E CSD10060G	DPA	Per spec	10	462	0

External optical inspection was performed at 40X magnification after samples were preconditioned to MSL3 and exposed to the reliability tests of Table 13. External optical inspection detected no defects.

Destructive Physical Analysis (DPA) resulted in the following conclusions:

- No delamination on the active side of the die.
- No delamination change >10% on any wire bonding surface of the die paddle.
- No delamination change >10% along any polymeric film bridging any metallic features that are designed to be isolated.
- No delamination/cracking change >10% through the die attach region for devices that require electrical contact to the backside of the die.
- No surface-breaking feature delaminated over its entire length (e.g., lead fingers).

By the criteria of J-STD-020C, all parts therefore pass DPA. No electrical failures were observed.

## Reliability Testing and Failure Mode Analysis

Reliability testing was performed to estimate the long-term performance of the device, and to determine when “wear-out” will occur. By convention, wear-out is reached at the Median Time To Failure (MTTF) for a representative sampling of devices. Stress factors tested for this study were thermal acceleration and electric field acceleration under high temperature and high humidity conditions.

### Three-Temperature Life Testing

Wear-out reliability of SiC-related technology is limited by the survival of the ohmic contact. As shown in Figure 1, for Cree Schottky diodes operating continuously in forward bias at the maximum junction temperature of 175°C, the median time to failure for a SiC wear-out-related failure mode is  $6 \times 10^7$  hours (60% lower confidence limit =  $4.3 \times 10^7$  hours), far exceeding the design goal of 250 years. Each of the three points at high temperature represents 50 samples, and the star represents the estimated median lifetime at the data-sheet-specified maximum junction temperature.

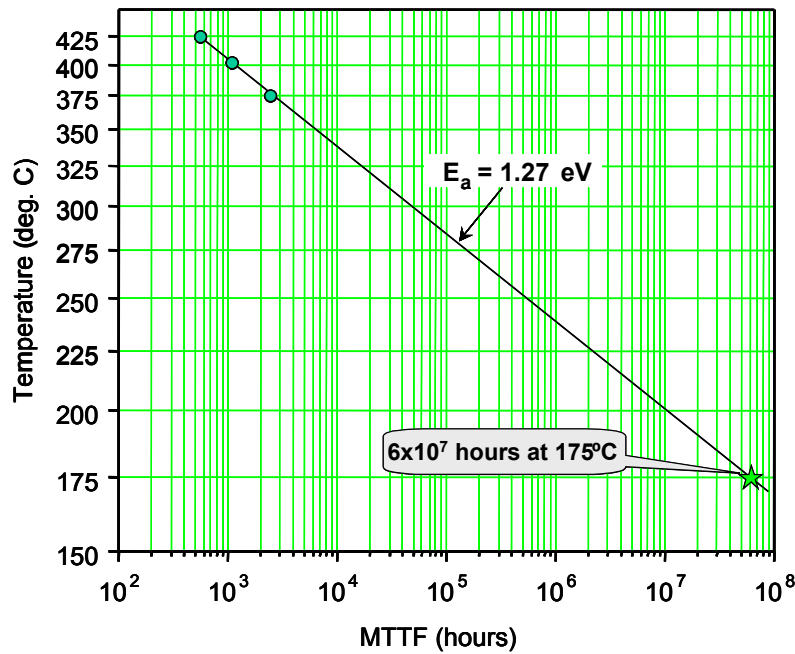
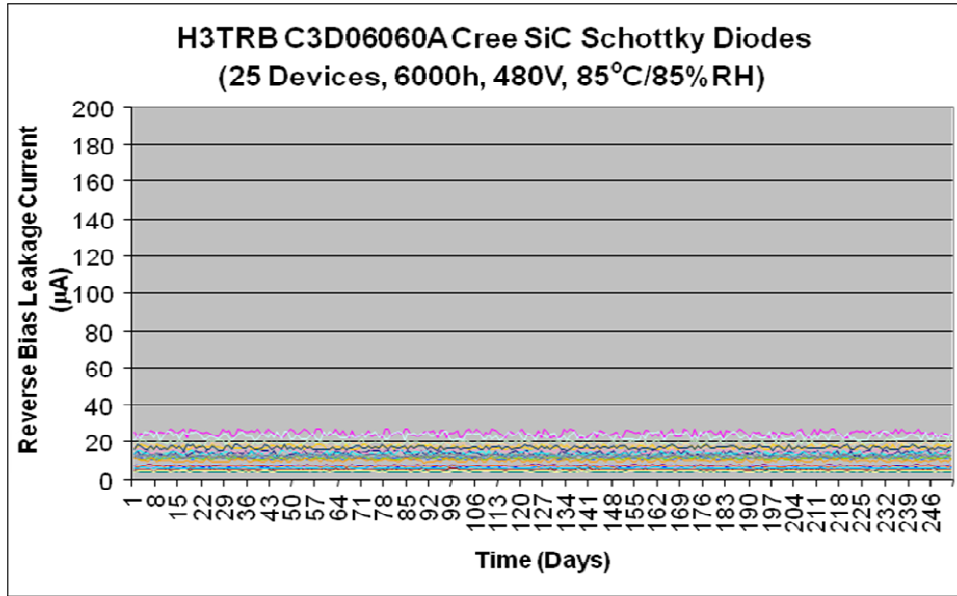


Figure 1: Arrhenius plot of accelerated-life test data

### Electric-Field and Moisture Accelerated Life Testing

A primary advantage of SiC for power electronics technology is its high breakdown field strength, which is 10 times higher than that of silicon. After four years in the field in both 1200-V and 600-V applications, and over 176 billion device hours in operation without a known SiC defect-related failure, Cree is confident that breakdown reliability of its SiC diode technology is not limited by materials or manufacturing quality. For the current generation of SiC devices, wear-out reliability due to high electric field is limited by the packaging material, but only under high heat and humidity conditions. Figure 2 shows in-situ data of the reverse bias leakage current at 480 V at 85°C and 85% Relative Humidity (RH). Twenty-five C3D06060A (TO-220-2 package style) devices were held for 6000 hours under these conditions, without failure.



**Figure 2: In-situ plot of accelerated electric field and moisture test data.**

After 6000 hours, the test was stopped, and Destructive Physical Analysis (DPA) was performed. No damage to the die, die metal structures, or die passivation was observed.



## Field Reliability and Failure Rate

Historically, Cree’s 600-V Schottky diode technology has demonstrated a high level of field quality and robustness. “FIT” is a statistical estimate of non-wearout failure rate and is expressed in “failures per billion device hours.” The collective FIT value for Cree’s SiC Schottky diode technology is 0.2, representing over 220 billion device hours in the field.

The assumptions made in calculating the FIT value are as follows: Product is in the field 60 days from shipment received, the product operates continuously for 12 hours per day, and 50% of field failures are reported to Cree.

The critical device structures of the Z-Rec product line (C3DXX060) are identical to those the CSDXX060 series of devices manufactured between 2004 and 2009 and are, therefore, expected to exhibit a similar FIT value in fielded applications. (A field failure related to the presence of a crystalline defect in SiC has not been observed since 2004.)

## Conclusion

Cree 600-V Schottky diodes were selected and tested as described in this report. The devices tested met all electrical performance requirements, and no failures were observed in any qualification test. Based on these results, the following Cree 600-V Schottky diode products are certified<sup>1†</sup> as qualified product according to Cree’s internal requirements.

C3D20060D		
C3D10060A	C3D10060F	C3D10060G <sup>†</sup>
C3D08060A	C3D08060F	C3D08060G <sup>†</sup>
C3D06060A	C3D06060F	C3D06060G <sup>†</sup>
C3D04060A	C3D04060E <sup>†</sup>	C3D04060F
C3D03060A <sup>†</sup>	C3D03060E <sup>†</sup>	C3D03060F <sup>†</sup>
C3D02060A	C3D02060E <sup>†</sup>	C3D02060F

Package Styles:

A=TO-220-2, D=TO-247-3, E=TO-252-2 “DPAK”, F=TO-220-2 “Full Pack”

<sup>†</sup>Qualified by similarity; surface-mount devices (E and G series) qualified to MSL-3

<sup>‡</sup> This report and its conclusions do not imply any guarantee, warranty, or suitability for any purpose regarding the products mentioned. Results represent the particular devices tested, which were randomly selected according to the sampling plan described herein.