# Drift-Free, 50 A, 10 kV 4H-SiC PiN Diodes with Improved Device Yields

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**Abstract.** The path to commericializing a 4H-SiC power PiN diode has faced many difficult challenges. In this work, we report a 50 A, 10 kV 4H-SiC PiN diode technology where good crystalline quality and high carrier lifetime of the material has enabled a high yielding process with $V_F$ as low as 3.9 V @ 100 A/cm$^2$. Furthermore, incorporation of two independent basal plane dislocation reduction processes (LBPD 1 and LBPD 2) have produced a large number of devices that exhibit a high degree of forward voltage stability with encouraging reverse blocking capability. This results in a total yield (forward, 10 kV blocking, and drift) of >20% for 8.7 mm x 8.7 mm power PiN diode chips—the largest SiC chip reported to date.

## Introduction

Rapid advancement of 4H-SiC PiN diode technology has enabled record high blocking voltage (up to 20 kV) with relatively low forward voltage drops ($V_F$) [1]. This is a direct consequence of improved crystal growth (reduced micropipe and defect density) and epitaxy (reduced epi defects and high minority carrier lifetimes) which permits full utilization of the large critical field and enhanced conductivity modulation. Despite such progress, the PiN diodes may suffer from significant forward voltage instability due to stacking faults spawned from basal plane dislocations (BPD) [2]. This problem is exacerbated with thick epitaxy because the faulted area scales with the drift layer thickness. Clearly, the reduction of BPDs is vital in developing a stable SiC PiN diode. Innovations in epitaxy have produced 100 μm drift layers with BPD densities of 10 cm$^{-2}$ and 20 cm$^{-2}$ for independent processes LBPD 1 and LBPD 2, respectively [3]. PiN diodes fabricated with LBPD 1 have already shown excellent $V_F$ stability across the wafer, but poor surface morphology reduced the reverse blocking yield to just 2% [4]. Recent optimization of the LBPD 1 process has improved the surface morphology while maintaining the low BPD density. In this contribution, we report the effect of incorporating standard (continuous growth of the $n^-$ drift and $p^+$ injector layers), improved LBPD 1, and LBPD 2 epitaxy in the 50 A, 10 kV 4H-SiC PiN diode process.

## Experimental

High quality epitaxial layers (100 μm drift layer, $N_D$ = 2E14 cm$^{-3}$, and 2 μm injection layer, $N_A$ = 8E18 cm$^{-3}$) are continuously grown on 0.6 cm$^{-2}$ micropipe density 8° off-axis (0001) 4HN conducting substrates. The devices are mesa isolated by etching down to the n- drift layer in the field areas. Next, an aluminum implanted guard ring-based termination is formed around the device periphery while a nitrogen implanted channel stop region grounds the field area away from the devices. The implants are activated with a 1600°C anneal in Ar. The surface is passivated with a silicon dioxide layer. Sintered Ti-Al and Ni contacts are made to the anode and cathode, respectively, before depositing thick Au overlayers. The 8.7 mm x 8.7 mm chip contains a single 50 A PiN diode (0.50 cm$^2$ active area), while a drop-in chip contains a 20 A PiN diode (0.20 cm$^2$ active area) and five small PiN diodes (0.0078 cm$^2$ active areas).

## Results

All three epitaxial processes yield PiN diodes with good blocking and low, stable $V_F$. Figure 1 shows the reverse blocking capability of a typical large diode. Reverse blocking is measured out to 9 kV where the leakage current exceeds the current compliance limit of the measurement apparatus. In terms of leakage current density, the 0.5 mA/cm$^2$ corresponds to a minimal value that is well below the typical current densities allowed in reverse operation. Hence, a 10 kV blocking is implied for the large devices blocking >7 kV. A low forward voltage drop of 3.9 V is observed at 50 A (100 A/cm$^2$) indicating a high degree of conductivity modulation (Fig. 2). PiN diodes are capable of handling very high current densities and we have measured this large device out to a pulsed current of 328 A (656 A/cm$^2$) at a low forward drop of 5.9 V. For a single chip, this demonstrates over 3 MW of pulsed power! These devices also show excellent forward characteristics with respect to temperature (Fig. 3). The $V_F$ at low current densities decreases slightly due to temperature enhanced carrier lifetime which is a concern for thermal runaway. However, at high current densities, the behavior reverses to a positive temperature coefficient with a zero temperature coefficient observed at 400 A/cm$^2$, thereby making these devices attractive for use in a parallel configuration where the current must be properly shared.

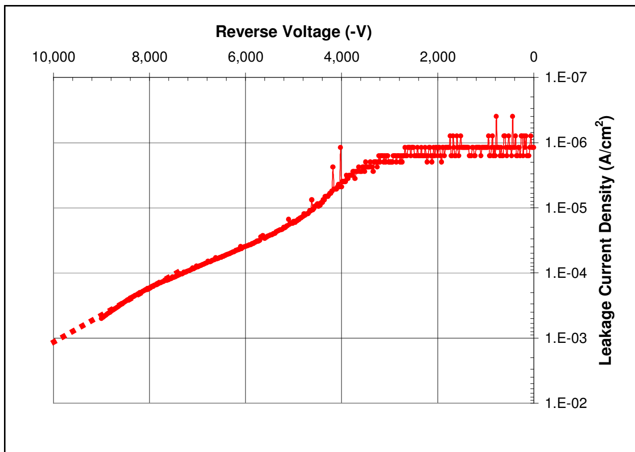


Fig. 1. Reverse J-V characteristic of a 50 A diode (8.7 mm x 8.7 mm) showing >9 kV blocking (solid curve) that is current compliance limited. The dashed line extrapolates the reverse blocking to 10 kV.

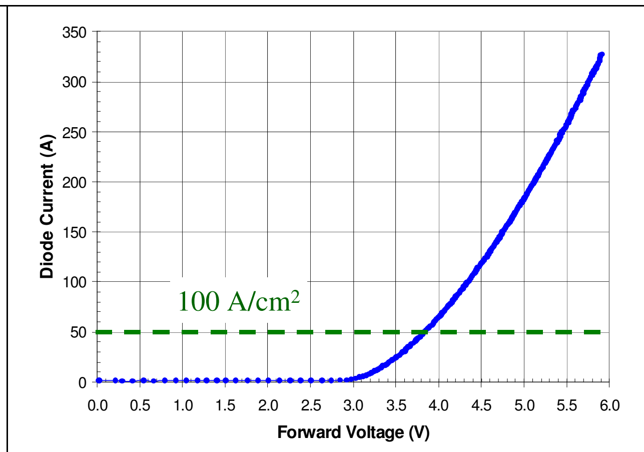


Fig. 2. Pulsed forward I-V characteristic of a large 10 kV diode with a 3.9 V forward drop at 50 A and 5.9 V forward drop at 328 A indicating a high level of conductivity modulation.

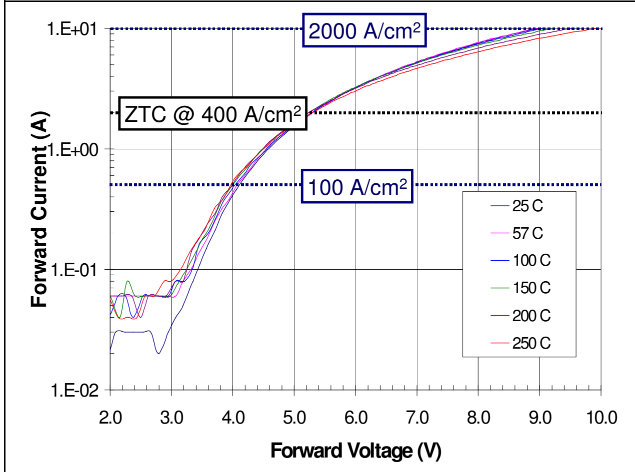


Fig. 3. Forward I-V curve measured at several temperatures on a small 10 kV device where a positive temperature coefficient facilitates device paralleling.

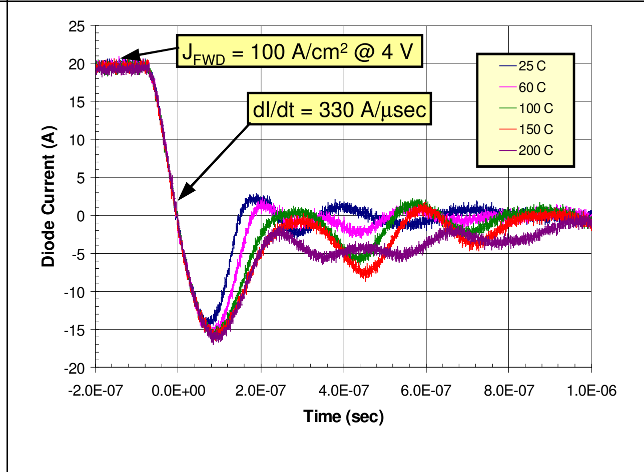


Fig. 4. Large dI/dt reverse recovery transient showing fast turn-off with very little reverse recovery charge for a 20 A, 10 kV device.

The low forward voltage drops obtained on these devices are derived from high carrier lifetimes that increase the conductivity of the nominally high resistance drift layer. One potential drawback is that the switching ability may suffer, especially the turn-off transient, due to the extra time needed for carrier removal in the drift layer. The reverse recovery of the 20 A, 10 kV diodes (Fig. 4) shows a fast ~200 nsec recovery with very little reverse recovery charge despite an aggressive dI/dt of 330 A/µsec.

To be a commercially viable product, good device performance must be demonstrated across the entire wafer. Figure 5 illustrates the 10 kV blocking wafermaps for the three epitaxial splits (please recall the aforementioned discussion regarding the implied 10 kV blocking for devices leaking 300 µA at >7 kV). As expected, the standard epitaxy and the relatively benign LBPD 2 processes give the best yields of 37% and 35%, respectively. Although the more aggressive LBPD 1 process shows a lower yield of 27%, this is still a substantial improvement over our previous attempt where the blocking yield was a mere 2%. Key yield limiters appear to be particles and defects generated in the epigrowth as well as the ability to fully resolve the guard ring photolithography across the wafer. Overcoming these limitations should increase the reverse blocking yield to well over 50%.

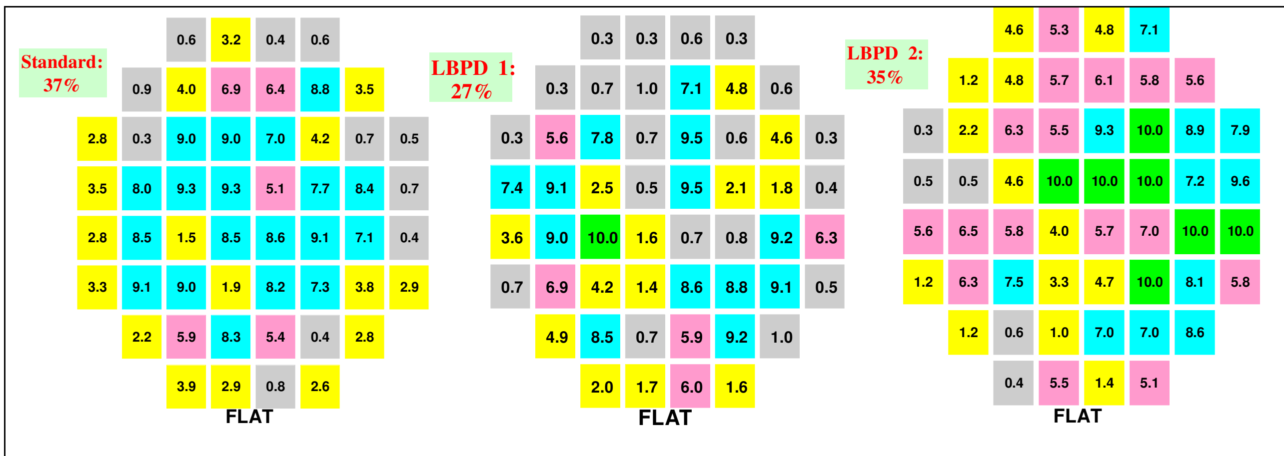


Fig. 5. Reverse blocking wafermaps showing the blocking voltage at 300 µA leakage current. Due to this low current compliance, we are unable to measure the devices to their full blocking capability, hence 10 kV blocking is implied for >7 kV devices (blue and green).

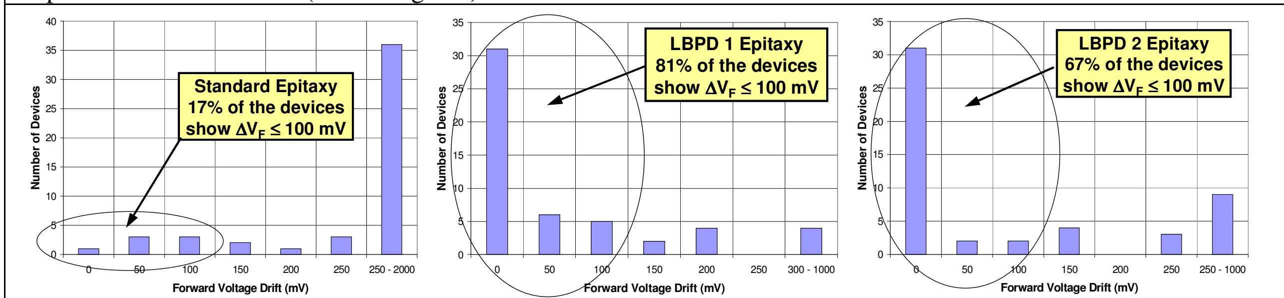


Fig. 6. Forward voltage drift histograms for the three epitaxial processes. Both LBPD processes show dramatic improvement in the 100 mV drift yield

In the forward operation, the initial $V_F$ measured across the wafer is very uniform. The more discriminating test is to measure the stability of the forward voltage. With the advent of continuous growth epitaxy, the diodes have become more well behaved such that they may be screened with a simple on-wafer stress measurement: 1.) measure pulsed initial $V_F$ @ 50 A/cm$^2$ at room temperature; 2.) constant current stress at 50 A/cm$^2$ for 30 min which also heats the device; 3.) cool down to room temperature; 4.) measure pulsed final $V_F$ @ 50 A/cm$^2$; 5.) move to next die on wafer and repeat until the entire wafer is tested. Histograms in Fig. 6 illustrate the number of stable

devices by binning the devices according to the amount of forward voltage increase. Using 100 mV as an acceptable amount of $V_F$ drift, we observe $V_F$ drift yields of 17%, 81%, and 67% for the standard, LBPD 1, and LBPD 2, respectively. These numbers are consistent with the observed occurrence of BPDs in the epitaxy and demonstrate that a large number of stable devices can be manufactured per wafer.

## Summary

Isolated hero devices have been historically reported by many groups. Our emphasis, however, is to take this one step further and make the hero devices the norm, rather than the exception, on the wafer. Table 1 shows our progress toward this goal. From the 20 A experiment, we demonstrated two processes that dramatically increased the drift yield. However, the LBPD 1 process had poor blocking yield due to surface morphology issues. In the ensuing 50 A experiment, we optimized the LBPD 1 process to improve the surface morphology, thereby giving us two independent 4H-SiC PiN diode processes capable of yielding >20% of the 8.7 mm x 8.7 mm chips (the largest SiC chip reported to date). This trend of making the large hero devices more common on the wafer is a significant step in the evolution of a commerically viable SiC PiN diode technology expected to meet the demands of high voltage, high frequency power conversion applications.

Table 1. Improved device yields corresponding to historical improvements in thick epitaxy

| Epitaxy | BPD ($cm^{-2}$) | Device | Drift Yield | 10 kV Yield | Total Yield |
|---|---|---|---|---|---|
| 2 Step Growth | 300 | 7.5 A | 0 % | 10 % | 0 % |
| Standard 1 Growth | 180 | 20 A | 15 % | 40 % | 6 % |
| Original LBPD 1 | 10 | 20 A | 86 % | 2 % | 2 % |
| Original LBPD 2 | 20 | 20 A | 67 % | 39 % | 26 % |
| **Standard 1 Growth** | **180** | **50 A** | **17 %** | **37 %** | **6 %** |
| **Improved LBPD 1** | **10** | **50 A** | **81 %** | **27 %** | **22 %** |
| **Original LBPD 2** | **20** | **50 A** | **67 %** | **35 %** | **23 %** |

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