

# Highly Efficient Operation Modes in GaN Power Transistors Delivering Upwards of 81% Efficiency & 12W Output Power

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*Development of a 'first-pass' inverse class-F design procedure has obtained very high efficiency device performance, at high power levels...*

## The Motivation – High Efficiency PA Modes

- Require a systematic design and realisation process to overcome time-consuming and multi-iterative PA designs
- Design of complex PA modes → Requirement for harmonic characterisation / measurement capability
- Need a process for rapidly optimising harmonic impedances

## The Solution – A Process for Rapid PA Optimisation

- Methodology has been developed for an effective, working design approach
- Utilising Cardiff University's time-domain waveform measurement capability to engineer high efficiency waveforms and device performance
- First pass design success, provided good prior stability analysis
- Approaching theoretical optimum efficient device performance - 84.0% efficiency obtained at 2.1GHz operating with 40V DC rail

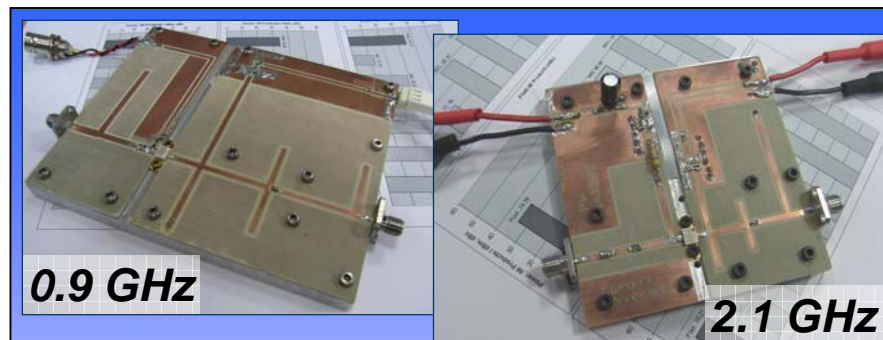
### High power device characterisation/waveform engineering

- A real measure of device performance intended for PA applications

Process has successfully yielded TWO 10W+ amplifiers operating at 80%+ efficiency using this FAST design approach!

## Inverse class-F PA realisations

Extended work has made direct use of captured data for designs of complex PA modes → promising results following realisation of two high efficiency prototype PAs.



Performance Measures	Device Measurements (0.9GHz Fundamental)	Realised PA (0.9GHz Fundamental)
P1dB Output Power	38.6 dBm	38.1 dBm <b>(38.4dBm at the dev.)</b>
P3dB Output Power	40.6 dBm	40.4 dBm <b>(40.7dBm at the dev.)</b>
Max. Avail. Gain at P1dB	25.6 dB	24.2 dB <b>(24.5dB at the dev.)</b>
Drain Efficiency at P3dB	79.8 %	76.7 % <b>(82.2% at the dev.)</b>

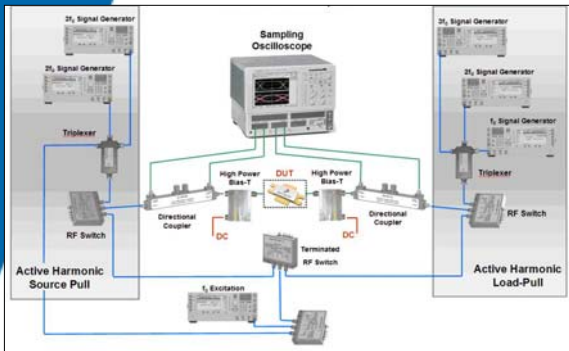
**Key Advantage:** Design does not require manufacturers non-linear device models!

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*RF waveform engineering was used to obtain high efficiency inverse class-F waveforms at the device current generator ( $I_{gen}$ ) plane...*

## Waveform Measurement System

Calibrated Time-Domain Waveform Measurements  
Active Load-Pull: Fundamental / Multi Harmonic

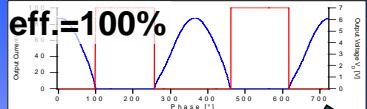


- Time domain RF waveform capture
- High power active load-pull capability
- Independent control of fundamental, 2<sup>nd</sup>, 3<sup>rd</sup> harmonic terminations

## Waveform Engineering Design Process

1. On-wafer techniques for optimising device performance have been adapted for use on high-power, packaged devices.
2. By modeling output and package parasitics, it is possible to de-embed to the device plane and engineer theoretical waveforms inside the package.
3. Perform high power measurements at calibrated package reference plane.
4. Verification of performance established and compared with theory, quickly.

## Inverse Class-F Theoretical Efficiencies



**Ideal waveforms**

### Wave Shaping

- 5-harmonic terms in current waveforms ( $I_{max}$  boundary)
- 2-harmonic terms in voltage waveform (active load-pull)

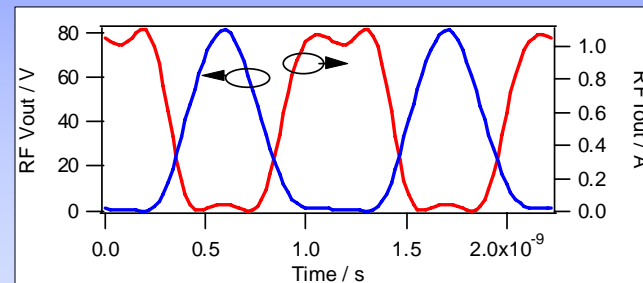
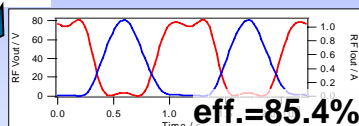
### Approximations

- Bandwidth limitation factors
- DC Offsets
- Ability to generate perfect loads

$$\eta_{voltage} \cdot \eta_{current} = 1.000 \times 0.854 = 0.854$$

$$\eta_{drain} = 100 \times \frac{V_{DC} - V_{knee}}{V_{DC}} \times 0.854$$

**Practical waveforms**



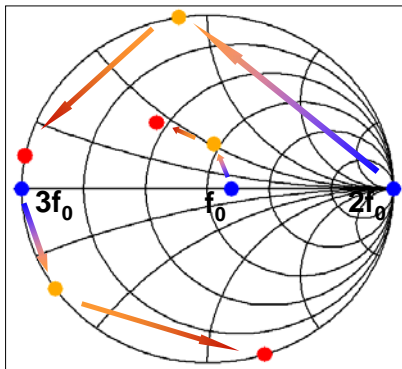
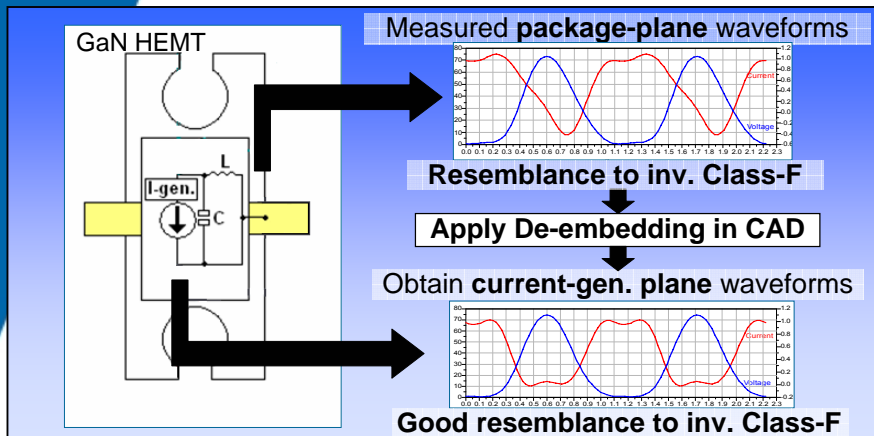
**10W GaN HEMT was used in this investigation to obtain high efficiency PA modes of operation, including inverse class-F.**

**Design procedure carried out at 0.9GHz AND 2.1GHz.**

# Highly Efficient Operation Modes in GaN Power Transistors Delivering Upwards of 81% Efficiency & 12W Output Power

*Drain efficiencies above 81% have been achieved at 0.9GHz and 2.1GHz for a wide band-gap gallium nitride (GaN) HEMT transistor and 12W fundamental output power...*

## Output Parasitic Modelling and De-embedding

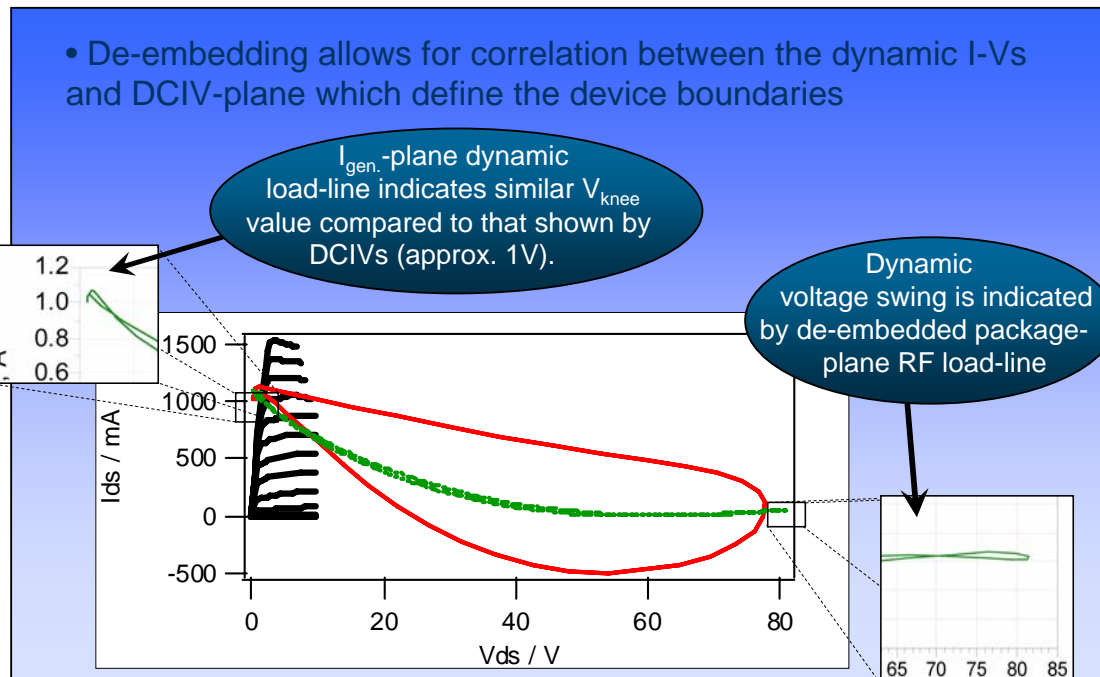


*Utilise output parasitic model in predicting optimum impedances at any frequency, e.g. to obtain inverse class-F operation at the  $I_{gen.}$ -plane.*

- $I_{gen.}$ -plane
- Package-plane 0.9GHz
- Package-plane 2.1GHz

## Device boundaries

*Voltage offset or “walkout” effect is minimised by operating at lower drain current → Same output power through increased drain voltage swing → 1V voltage offset (“knee”) in this study...*



- De-embedding allows for correlation between the dynamic I-Vs and DCIV-plane which define the device boundaries

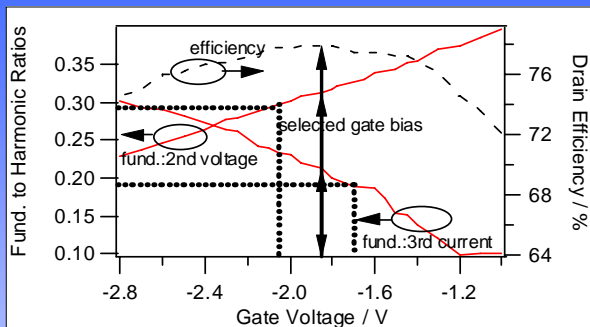
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*Investigations into improvements in drain efficiency through increases in drain bias voltage have yielded device drain efficiencies of up to 84% at 2.1GHz...*

## Performance Analysis at 0.9GHz

### Gate Bias Sweeps and Results at 0.9GHz:

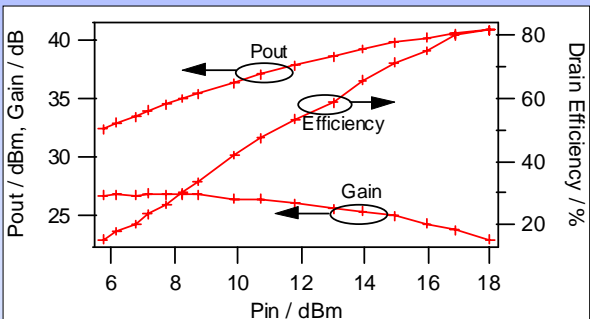
#### Gate bias sweep



#### Maximally-Flat Ratios

- Require fund:2<sup>nd</sup> - harm. voltage ratio of 0.29
- Require fund:3<sup>rd</sup> - harm. current ratio of 0.18
- Resulting gate voltage = -1.85V

#### Power sweep following optimisation



#### High Efficiency Performance

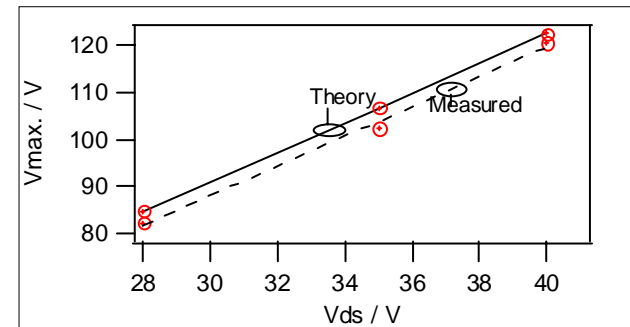
- 12Watts output power
- 22dB device gain.
- 81.5% drain efficiency

## Inverse Class-F Scaled to 2.1GHz AND up to Vds of 40V

- RF voltage swing and DC rail relationship shows good theoretical agreement, according to eq.  $\rightarrow V_{max.} = \pi \cdot (V_{DC} - V_{knee})$

#### High Efficiency GaN at 2.1GHz

- Design process scales with frequency.
- High device breakdown limits allow for extending  $V_{ds}$  well beyond 28V.
- Efficiency extends to 84%!



## Conclusions and Discussions

- Successful 'first-pass' designs is now a reality.
- Drain efficiencies of 84% have been obtained for optimised device operation at 2.1GHz operating with 40V DC rail  
 $\rightarrow$  Design procedure achieves scalable device performance!
- Waveform engineering is a powerful tool in design of complex PA modes and achieving theoretical optimum device performance.
- High output power and gain have not been compromised.